

IN THE CLAIMS:

Please cancel claim 72 without prejudice; and amend claims 1, 2, 7, 9, 10, 12 through 14, 17 through 19, 21, 22, 34, 37, 38, 42, 48, 49, 50, 52, 55, 56, 62, 65, 68, 70, 73, 77, 80, 81 and 84 to read as indicated below:

1 1. (currently amended) Apparatus for deterring failure of a  
2 computing system; said apparatus comprising:  
3 a hardware network of components, having substantially no  
4 software and substantially no firmware except programs held in an  
5 unalterable read-only memory;  
6 terminals of the network for connection to such system; and  
7 fabrication-preprogrammed hardware circuits of the network  
8 for guarding such system from such failure.

1 2. (currently amended) The apparatus of claim 1, particularly  
2 for use with such system that is substantially exclusively made  
3 up of commercial, off-the-shelf components; and wherein:  
4 at least one of the network terminals is connected to re-  
5 ceive at least one error signal generated by such system in event  
6 of incipient such failure of such system;  
7 at least one of the network terminals is connected to pro-  
8 vide at least one recovery signal to such system upon receipt of  
9 the error signal; and  
10 the apparatus further comprises means for automatically  
11 responding to the at least one error signal by generating the at  
12 least one recovery signal for guarding all of such system against  
13 such failure.

1 3. (previously presented) The apparatus of claim 1, wherein:  
2 the network is an infrastructure which is generic in that it  
3 can accommodate any such system that can issue an error message  
4 and handle a recovery command.

1 4. (original) The apparatus of claim 1, further comprising:  
2 such computing system.

1 5. (original) The apparatus of claim 1, wherein:  
2 the circuits comprise portions for identifying failure of  
3 any of the circuits and correcting for the identified failure.

1 6. (previously presented) The apparatus of claim 1, wherein:  
2 the circuits are not capable of running any application pro-  
3 gram.

1 7. (currently amended) The apparatus of claim 1, particularly  
2 for use with a computing system that is substantially exclusively  
3 made of commercial, off-the-shelf components and that has at  
4 least one hardware subsystem for generating a response of the  
5 system to failure; and wherein:  
6 the circuits comprise portions for reacting to such said re-  
7 sponse of such hardware subsystem.

1 8. (original) The apparatus of claim 1, particularly for use  
2 with a computing system that has plural generally parallel  
3 computing channels; and wherein:

4 the circuits comprise portions for comparing computational  
5 results from such parallel channels.

1 9. (currently amended) The apparatus of claim 8, wherein:

2 the parallel channels of such computing system are of di-  
3 verse design or manufacture origin.

1 10. (currently amended) The apparatus of claim 1, particularly  
2 for use with a computing system that has plural processors; and  
3 wherein:

4 the circuits comprise portions for identifying such failure  
5 of any of such processors and correcting for identified such  
6 failure.

1 11. (previously presented) The apparatus of claim 1, wherein:

2 the circuits comprise modules for collecting and responding  
3 to data received from at least one of the terminals, said modules  
4 comprising:

5  
6 at least three data-collecting and -responding modules,  
7 and

8  
9 processing sections for conferring among the modules to  
10 determine whether any of the modules has failed.

1 12. (currently amended) The apparatus of claim 1, particularly  
2 for use with a computing system that is substantially exclusively  
3 made of commercial, off-the-shelf components and that has at  
4 least one subsystem for generating a response of the system to  
5 failure, and that also has at least one subsystem for receiving  
6 recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and  
8 a corrective reaction between such the response-generating sub-  
9 system and such the command-receiving subsystem.

1 13. (currently amended) Apparatus for deterring failure of an  
2 entire computing system, wherein the computing system optionally  
3 includes plural mutually redundant modules; said apparatus  
4 comprising:

5 a network of components having terminals for connection to  
6 such system, wherein the network is constructed to be initially  
7 and permanently distinct from such computing system including all  
8 of such redundant modules if present; and

9 circuits of the network for operating programs to guard such  
10 entire system from such failure;

11 the circuits comprising portions for identifying such fail-  
12 ure of any of the circuits and correcting for the identified such  
13 failure.

1 14. (currently amended) The apparatus of claim 13, wherein:

2 the program-operating portions comprise a section that  
3 corrects for the identified such failure by automatically taking  
4 a failed circuit out of operation.

15. (previously presented) The apparatus of claim 13, wherein:  
the network is an infrastructure that continuously waits to  
respond to messages from such system.

1 16. (original) The apparatus of claim 13, further comprising:  
2 such computing system.

1 17. (currently amended) The apparatus of claim 13, wherein:  
2 the program-operating portions comprise at least three of  
3 the circuits; and  
4 such failure is identified at least in part by majority vote  
5 among the at least three circuits.

1 18. (currently amended) The apparatus of claim 13, wherein:  
2 to guard such entire system from failure, said circuits re-  
3 ceive from such system error messages warning of incipient such  
4 failure, and issue recovery commands to such system.

1 19. (currently amended) The apparatus of claim 13, particularly  
2 for use with a computing system that is substantially exclusively  
3 made of commercial, off-the-shelf components and that has at  
4 least one hardware subsystem for generating a response of the  
5 system to failure; and wherein:  
6 the circuits comprise portions for reacting to such said re-  
7 sponse of such hardware subsystem.

1 20. (original) The apparatus of claim 13, particularly for use  
2 with a computing system that has plural generally parallel com-  
3 puting channels; and wherein:  
4 the circuits comprise portions for comparing computational  
5 results from such parallel channels.

1 21. (currently amended) The apparatus of claim 16, wherein:  
2 the computing system has such parallel channels that are of  
3 diverse design ~~or origin~~.

[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIM 70,  
PREFERABLY FOR INSERTION HERE.]

1 22. (currently amended) The apparatus of claim 13, particularly  
2 for use with a computing system that has plural processors; and  
3 wherein:  
4 the circuits comprise portions for identifying such failure  
5 of any of such processors, based on error messages from such sys-  
6 tem, and for correcting for identified such failure.

1 23. (previously presented) The apparatus of claim 13, wherein:  
2 the network is an infrastructure which is generic in that it  
3 can accommodate any such system that can issue an error message  
4 and handle a recovery command.

1 24. (previously presented) The apparatus of claim 13, particu-  
2 larly for use with a computing system that is substantially  
3 exclusively made of commercial, off-the-shelf components and that  
4 has at least one subsystem for generating a response of the  
5 system to failure, and that also has at least one subsystem for  
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and  
8 a corrective reaction between such response-generating subsystem  
9 and such command-receiving subsystem.

25. - 32. (canceled)

1 33. (previously presented) Apparatus for deterring failure of a  
2 computing system that is substantially exclusively made of com-  
3 mercial, off-the-shelf components and that has at least one hard-  
4 ware subsystem for generating an error message of the system  
5 about incipient failure; said apparatus comprising:

6 a network of components having terminals for connection to  
7 such system; and

8 circuits of the network for operating programs to guard such  
9 system from failure;

10 the circuits comprising portions for reacting to such error  
11 message of such hardware subsystem.

1 34. (currently amended) The apparatus of claim 33, wherein:

2 in response to such error message, the circuits guard the  
3 entire such system from failure.

1 35. (previously presented) The apparatus of claim 33, wherein:  
2 the network is generic in that it can accommodate any such  
3 system that can issue an error message and handle a recovery  
4 command.

1 36. (original) The apparatus of claim 33, further comprising:  
2 such computing system, including such hardware subsystem.

1 37. (currently amended) The apparatus of claim 36, wherein:  
2 the computing system has plural generally parallel computing  
3 channels; and  
4 such the parallel channels of the computing system are of  
5 diverse design or manufacture origin.

1 38. (currently amended) The apparatus of claim 33, wherein:  
2 said circuits are not capable of operating any application  
3 program; and are not controlled by any associated host computer  
4 that is capable of running any application program.

39. and 40. (canceled)

1 41. (previously presented) The apparatus of claim 33, particu-  
2 larly for use with a computing system that is substantially  
3 exclusively made of commercial, off-the-shelf components and that  
4 has at least one subsystem for generating a response of the  
5 system to failure, and that also has at least one subsystem for  
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and  
8 a corrective reaction between such response-generating subsystem  
9 and such command-receiving subsystem.

1 42. (currently amended) Apparatus for deterring failure of an  
2 entire computing system that is distinct from the apparatus and  
3 that has plural generally parallel computing channels and has at  
4 least one application-data input module, and at least one  
5 processor for running an application program; said apparatus  
6 comprising:

7 a network of components having terminals for connection to  
8 such system; and

9 circuits of the network for operating programs to guard such  
10 entire system from such failure, wherein the network is con-  
11 structed to be initially and permanently distinct from such  
12 computing system including substantially (a) every such applica-  
13 tion-data input module and (b) every such application-program  
14 processor, and (c) all of such parallel computing channels;

15 the circuits comprising portions for comparing computational  
16 results from such parallel channels.

1 43. (original) The apparatus of claim 47, wherein:  
2 the parallel channels of the computing system are of diverse  
3 design or origin.

1 44. (original) The apparatus of claim 42, wherein:  
2 the comparing portions comprise at least one section for  
3 analyzing discrepancies between the results from such parallel  
4 channels.

1 45. (previously presented) The apparatus of claim 44, wherein:  
2 the circuits are not capable of running any application pro-  
3 gram.

1 46. (previously presented) The apparatus of claim 42, wherein:  
2 the network is an infrastructure which is generic in that it  
3 can accommodate any such system that can issue an error message  
4 and computational results, and handle a recovery command.

1 47. (original) The apparatus of claim 42, further comprising:  
2 such computing system.

1 48. (currently amended) The apparatus of claim 42, wherein:  
2 the circuits do not and cannot operate any application  
3 program; and are not controlled by any associated host computer  
4 that is capable of running any application program.

1 49. (currently amended) The apparatus of claim 48, wherein:  
2 to guard such entire system from such failure, the circuits  
3 receive from such computing system error messages warning of in-  
4 cipient such failure and issue recovery commands to such comput-  
5 ing system.

1 50. (currently amended) Apparatus for deterring failure of an  
2 entire computing system that is distinct from the apparatus and  
3 that has plural generally parallel computing channels; said ap-  
4 paratus comprising:  
5 a network of components having terminals for connection to  
6 such system; and  
7 circuits of the network for operating programs to guard such  
8 entire system from such failure, wherein such network is con-  
9 structed to be initially and permanently distinct from such com-  
10 puting system including all of such parallel computing channels;  
11 the circuits comprising portions for comparing computational  
12 results from such parallel channels; and wherein:  
13 the comparing portions comprise circuitry for performing an  
14 algorithm to validate a match that is inexact; and  
15 the algorithm-performing circuitry employs a degree of inex-  
16 actness suited to a type of computation under comparison.

1 51. (previously presented) The apparatus of claim 50, wherein:  
2 the algorithm-performing circuitry performs an algorithm  
3 that selects a degree of inexactness based on type of computation  
4 under comparison; and  
5 the circuits also impose corrective action upon such system  
6 based upon discrepancies found by the comparing portions.

[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIM 71 THROUGH 74,  
PREFERABLY FOR INSERTION HERE.]

1 52. (currently amended) The apparatus of claim 42, particularly  
2 for use with a computing system that has plural processors; and  
3 wherein:

4 the circuits comprise portions for identifying such failure  
5 of any of such processors and correcting for identified such fai-  
6 lure.

1 53. (original) The apparatus of claim 42, wherein:

2 the circuits comprise modules for collecting and responding  
3 to data received from at least one of the terminals, said modules  
4 comprising:

5  
6 at least three data-collecting and -responding modules,  
7 and

8  
9 processing sections for conferring among the modules to  
10 determine whether any of the modules has failed.

1 54. (previously presented) The apparatus of claim 42, particu-  
2 larly for use with a computing system that is substantially  
3 exclusively made of commercial, off-the-shelf components and that  
4 has at least one subsystem for generating a response of the  
5 system to failure, and that also has at least one subsystem for  
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and  
8 a corrective reaction between such response-generating subsystem  
9 and such command-receiving subsystem.

1 55. (currently amended) Apparatus for deterring failure of any  
2 computing system that has plural processors and has at least one  
3 application-data input module, and at least one processor for  
4 running an application program, and is capable of generating an  
5 error message warning of incipient failure and capable of re-  
6 sponding to a recovery command; said apparatus comprising:

7 a network of components having terminals for connection to  
8 such system, wherein the network is constructed to be initially  
9 and permanently distinct from such any computing system including  
10 substantially (a) every such application-data input module and  
11 (b) every such application-program processor, and (c) all of such  
12 plural processors; and

13 circuits of the network for operating programs to guard any  
14 such system from such failure;

15 the circuits comprising portions for identifying such fail-  
16 ure of any of such processors and correcting for identified such  
17 failure.

[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIM 75,  
PREFERABLY FOR INSERTION HERE.]

1 56. (currently amended) The apparatus of claim 75, wherein:  
2 the identifying portions comprise a section that corrects  
3 for the identified such failure by taking a failed processor out  
4 of operation.

57. (previously presented) The apparatus of claim 75, wherein:  
the circuits cannot and do not run an application program.

1 58. (previously presented) The apparatus of claim 75, wherein:  
2 the circuits protect the entire such computing system.

1 59. (previously presented) The apparatus of claim 75, further  
2 comprising:  
3 such computing system.

60. (canceled)

1 61. (previously presented) The apparatus of claim 75, par-  
2 ticularly for use with a computing system that is substantially  
3 exclusively made of commercial, off-the-shelf components and that  
4 has at least one subsystem for generating a response of the  
5 system to failure, and that also has at least one subsystem for  
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and  
8 a corrective reaction between such response-generating subsystem  
9 and such command-receiving subsystem.

1 62. (currently amended) Apparatus for deterring failure of an  
2 entire computing system that is distinct from the apparatus and  
3 has at least one application-data input module, and at least one  
4 processor for running an application program; said apparatus  
5 comprising:  
6 a network of components having terminals for connection to  
7 such system; and  
8 circuits of the network for operating programs to guard such  
9 entire system from such failure;  
10 the circuits comprising modules for collecting and respond-  
11 ing to data received from at least one of the terminals, said  
12 modules comprising:  
13  
14 at least three data-collecting and -responding modules,  
15 and  
16  
17 processing sections for conferring among the modules to  
18 determine whether any of the modules has failed;  
19  
20 wherein the network, including all of the modules and sub-  
21 stantially (a) every such application-data input module and (b)  
22 every such application-program processor, and (c) all of the  
23 processing sections, is constructed to be initially and perma-  
24 nently distinct from such computing system.

1 63. (original) The apparatus of claim 62, further comprising:  
2 such computing system.

1 64. (original) The apparatus of claim 62, particularly for use  
2 with a computing system that is substantially exclusively made of  
3 commercial, off-the-shelf components and that has at least one  
4 subsystem for generating a response of the system to failure, and  
5 that also has at least one subsystem for receiving recovery  
6 commands; and wherein:

7 the circuits comprise portions for interposing analysis and  
8 a corrective reaction between such response-generating subsystem  
9 and such command-receiving subsystem.

[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIMS 76 THROUGH 78,  
PREFERABLY FOR INSERTION HERE.]

1 65. (currently amended) Apparatus for deterring failure of a  
2 computing system that is substantially exclusively made of com-  
3 mercial, off-the-shelf components and that has at least one  
4 subsystem for generating a response of the system to failure, and  
5 that also has at least one subsystem for receiving recovery  
6 commands; said apparatus comprising:

7 a network of components having terminals for connection to  
8 such system between the response-generating subsystem and the  
9 recovery-command-receiving subsystem; and

10 circuits of the network for operating programs to guard such  
11 system from such failure;

12 the circuits comprising portions for interposing analysis  
13 and a corrective reaction between the response-generating sub-  
14 system and the command-receiving subsystem.

1 66. (previously presented) The apparatus of claim 65, further  
2 comprising:  
3 such computing system.

1 67. (previously presented) The apparatus of claim 65, wherein:  
2 the circuits cannot and do not run any application program.

1 68. (currently amended) The apparatus of claim 65, wherein:  
2 by responding to an error signal from such system, the  
3 circuits protect the entire such system from failure.

1 69. (previously presented) The apparatus of claim 65, wherein:  
2 the network is an infrastructure which is generic in that it  
3 can accommodate any such system that can issue an error message  
4 and handle a recovery command.

1 70. (currently amended) The apparatus of claim 13, wherein:  
2 the circuits do not and cannot operate any application pro-  
3 gram; and are not controlled by any associated host computer that  
4 is capable of running any application program.

1 71. (previously presented) The apparatus of claim 50, wherein:  
2 the circuits cannot and do not run any application program.

72. (canceled)

1 73. (currently amended) The apparatus of claim 50, wherein:  
2 to guard such entire system from failure, the circuits  
3 receive from such computing system error messages warning of  
4 incipient failure and issue recovery commands to such computing  
5 system.

1 74. (previously presented) The apparatus of claim 50, wherein:  
2 the network is an infrastructure which is generic in that it  
3 can accommodate any such system that can issue an error message  
4 and computational results, and can handle a recovery command.

1 75. (previously presented) The apparatus of claim 55, wherein:  
2 the program-operating circuits guard any such system from  
3 failure by issuing a recovery command; and  
4 the failure-identifying and correcting portions provide the  
5 recovery command.

1 76. (previously presented) The apparatus of claim 62, wherein:  
2 the circuits cannot and do not run any application program.

1 77. (currently amended) The apparatus of claim 62, wherein:  
2 to guard the entire such system from failure, the circuits  
3 receive from such computing system error messages warning of in-  
4 ipient failure ~~protect the entire such system.~~

1 78. (previously presented) The apparatus of claim 62, wherein:  
2 the network is an infrastructure which is generic in that it  
3 can accommodate any such system that can issue an error message  
4 and handle a recovery command.

1 79. (previously presented) The apparatus of claim 1, wherein:  
2 the apparatus is not a circuit breaker.

1 80. (currently amended) The apparatus of claim 1, wherein:  
2 at least one of the network terminals is connected to re-  
3 ceive at least one error signal generated by such system in event  
4 of incipient such failure of such system;  
5 at least one of the network terminals is connected to pro-  
6 vide at least one recovery signal to such system upon receipt of  
7 the error signal.

1 81. (currently amended) An infrastructure for a computing  
2 system that has at least one computing node ("C-node") for  
3 running at least one application program; said infrastructure  
4 being for guarding the system against failure, and comprising:  
5 at least one monitoring node ("M-node") for monitoring the  
6 condition of the at least one C-node by waiting for an error sig-  
7 nal, indicating incipient such failure, from the at least one C-  
8 node and responding to the error signal by sending a recovery  
9 command to the at least one C-node; and  
10 at least one adapter node ("A-node") for transmitting the  
11 error signal and recovery command between the at least one C-node  
12 and at least one M-node; and wherein:  
13 the at least one M-node is manufactured, and remains, wholly  
14 distinct from the at least one C-node; and  
15 the at least one M-node cannot, and does not, run any appli-  
16 cation program.

1 82. (previously presented) The infrastructure of claim 81,  
2 further comprising:  
3 such computing system.

1 83. (previously presented) The infrastructure of claim 81,  
2 particularly for use with such computing system that has plural  
3 such C-nodes; and further comprising:  
4 a decision-making node ("D-node") for comparing output data  
5 generated by such plural C-nodes and reporting to the at least  
6 one M-node any discrepancy between the output data; and wherein:  
7 the at least one M-node analyzes the D-node reporting, and  
8 based thereon arbitrates among the C-nodes.

1 84. (currently amended) An [[The]] infrastructure of claim 81,  
2 further for a computing system that has at least one computing  
3 node ("C-node") for running at least one application program;  
4 said infrastructure being for guarding the system against fai-  
5 lure, and comprising:  
6 at least one monitoring node ("M-node") for monitoring the  
7 condition of the at least one C-node by waiting for an error sig-  
8 nal, indicating incipient such failure, from the at least one C-  
9 node and responding to the error signal by sending a recovery  
10 command to the at least one C-node;  
11 at least one adapter node ("A-node") for transmitting the  
12 error signal and recovery command between the at least one C-node  
13 and at least one M-node; and wherein:  
14  
15 the at least one M-node is manufactured, and remains,  
16 wholly distinct from the at least one C-node, and  
17  
18 the at least one M-node cannot, and does not, run any  
19 application program; and  
20  
21 at least one self-checking node for startup, shutdown and  
22 survival ("S3-node"), specifically for executing power-on and  
23 power-off sequences for such system and for the infrastructure,  
24 and for receiving error signals and sending recovery commands to  
25 the at least one M-node.